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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,568	10/31/2002	Kuo-Ming Chen	NAUP0482USA	7641

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
LEBENTRITT, MICHAEL	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 01/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/065,568	CHEN ET AL.	
	Examiner	Art Unit	
	Michael S. Lebentritt	2824	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Beddingfield, US Patent 5,977,632.

Beddingfield discloses providing a semiconductor wafer(10), which comprises a substrate (10), an integrated circuit (not shown), and at Least one bump pad (12)formed on the substrate and electrically connected with the integrated circuit', forming a first dielectric Layer (16) on a surface of the bump pad; performing an etching process to form a contact hole in the first dielectric layer (figure 1) and to expose a portion of the bump pad (12) ; forming a second dielectric layer (18) on a surface of the semiconductor wafer outside of the contact hole, performing an under bump metallurgy (UBM) process so as to form a metal layer (24) on a surface of the contact hole; forming a solder bump (26) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board (figure 7). Please see figures 1-7 and discussion on column 2, line 35 to column 4, and line 35.

Also in regards to claim 6 wherein the second dielectric layer is composed of insulating materials. such as benocyclobutene (BCB), polyimide (PI), and BCB+PI (column 3, lines 5 to 15.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield as applied to claims 1 and 6 above, and Applicant's Admitted Prior Art (AAPA).

Beddingfield is applied supra but lacks the anticipation wherein the semiconductor wafer further comprises'. a plurality of fuses electrically connected with the integrated circuit; at Least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses a semiconductor wafer 1 0 comprises a substrate 1 2, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 1 2 further comprises a bump pad 1 4, a plurality of fuses 1 6, and an alignment key 1 8.The bump pad 1 4 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 1 4. In view of this

disclosure it would of been obvious to one of ordinary skill in the art at the time of invention to form a plurality of fuses electrically connected with the integrated circuit; at Least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Beddingfield, because the alignment key provides a means for visual inspection and the fuse provide electrical connection for probe testing.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield as applied to claims 1 and 6 above, and further in view of Liu et al, US Patent 6,395,622.

Beddingfield is applied supra but lacks the anticipation of wherein the circuit probing and an laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Liu discloses circuit probing and an laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. See figures 3c and 3d and discussion on column 3, line 30 to 60. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically

connecting with the solder bump as taught by Liu et al, because by testing after bumping and before laser repair the throughput is increased.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 7-9 are rejected under 35 U.S.C. 102(a) as being anticipated by AAPA

AAPA discloses, the semiconductor wafer 1 0 comprises a substrate 1 2, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 1 2 further comprises a bump pad 1 4, a plurality of fuses 1 6, and an alignment key 1 8.The bump pad 1 4 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 1 4. The fuses 1 6 are formed on an upper layer of the integrated circuit region and electrically connected with the embedded.
memory, and after finding invalid memory cells, word lines, or conducting wires within the embedded memory by performing a circuit probing process, a laser repair process is performed to eliminate these invalid elements by cutting off the corresponding fuses.

The prior art method is first forming a first dielectric layer 20 on the surface of the semiconductor wafer 1 0, which completely covers the bump pad 1 4 and the fuses 1 6. The first dielectric layer 20 is also called a passivation layer and is used to seal up and to avoid moistness. Thereafter, a photo-etching-process (PEP) is performed to form a contact hole 2 1 in the first dielectric layer 20 above the bump pad 1 4 so as to expose portions of the bump pad 1 4. Because a subsequent laser repair process uses laser beams to penetrate and to cut off portions of the fuses 1 6, the first dielectric layer 20 - must be composed of transparent materials. As shown in Fig.2, a circuit probing . - process is then performed, which uses a probing tip (not shown) electrically connected to the bump pad 1 4 to find invalid memory cells, word lines, or conducting wires within the embedded memory in the integrated circuit region, and the alignment key ' 1 8 is used to define the regions needed to accept laser repair. After that, an accurate laser zip process is performed to cut off portions of the fuses 1 6 in the regions defined by the alignment key 1 8 so as to destroy electrical connections of these invalid elements. As shown in Fig.3, a second dielectric layer 22 composed of benzocyclobutene (BCB), polyimide (PI), or BCB+PI is formed on the surface of the semiconductor wafer 1 0. Then, as shown in Fig.4, an under bump metallurgy (UBM) process is performed to form a metal layer 24, which is composed of specific multi-layer metal films, on a surface of the contact hole 2 1 by sputtering. The functions of the metal layer 24 comprise providing adhesion and diffusion barrier, improving moistness of the bump pad 1 4, and preventing oxidation. A solder bump 26 is then formed on the metal layer 24 corresponding to the contact hole 2 1 by evaporating, printing, electro-plating, dipping,

or ultrasonic soldering. Finally, the semiconductor wafer 1 0 is placed on a packaging board (not shown), and the solder bump 26 melted by a thermal treatment

Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Loo et al, US Patent 6,118,180.

Loo discloses providing a semiconductor wafer (400), which comprises a substrate, an integrated circuit, and at Least one bump pad (402) formed on the substrate and electrically connected with the integrated circuit-, forming a dielectric layer (406) on a surface of the bump pad; performing an etching process to form a contact hole in the dielectric layer (figure 6) and ' to expose a portion of the bump pad; performing an under bump metallurgy (UBM) process so as to form a metal layer (408) on a surface of the contact hole; forming a solder bump (412) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board. See figures 3-6 and discussion on column 5, line 30 to column 8, line 15.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loo et al as applied to claim 7 above, and Applicant's Admitted Prior Art (AAPA).

Loo is applied supra but lacks the anticipation wherein the semiconductor wafer further comprises'. a plurality of fuses electrically connected with the integrated circuit; at Least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses a semiconductor wafer 1 0 comprises a substrate 1 2, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 1 2 further

comprises a bump pad 1 4, a plurality of fuses 1 6, and an alignment key 1 8.The bump pad 1 4 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 1 4. In view of this disclosure it would of been obvious to one of ordinary skill in the art at the time of invention to form a plurality of fuses electrically connected with the integrated circuit; at Least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Loo, because the alignment key provides a means for visual inspection and the fuse provide electrical connection for probe testing.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loo as applied to claims 7, and further in view of Liu et al, US Patent 6,395,622.

Loo is applied supra but lacks the anticipation of wherein the circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Liu discloses circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. See figures 3c and 3d and discussion on column 3, line 30 to 60. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with

the solder bump as taught by Liu et al, because by testing after bumping and before laser repair the throughput is increased.

Conclusion

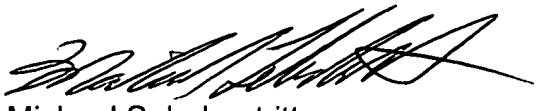
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen et al, US Patent 6,636,313 disclose forming a plurality of (mis) alignment marks (16) on a surface of the substrate (12) with an under bump pad (14). If the test piece passes the misalignment tolerance, a layer of under bump metallization (40,42) is deposited on top of said pad (14) and a solder bump (46) is then deposited upon the under bump metallization. Please see figures 1-5 and discussion on column 7, liner 25 to column 9, line 4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. Lebentritt whose telephone number is 571-272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-3431.



Michael S. Lebentritt

Primary Examiner
Art Unit 2824

January 20, 2004